AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 5, line 32, with the following rewritten paragraph:

Although being based on a similar technological concept ~~with~~ to the structure of Fig. 3 ~~in~~ with respect to the fact that the contact holes are narrowed by using the sidewalls, the structure shown in Fig. 4 has an advantage in that a smaller contact area can be provided than the structure of Fig. 3 by increasing the thickness of the sidewall as a result of depositing the first dielectric film 242 together with the sacrificial layer 244. However, additional steps, such as depositing the first dielectric film, depositing the sacrificial layer, etching the sacrificial layer and etching the first dielectric film, are required so that the process is more ~~complicate~~ complicated. Therefore, high productivity in manufacturing cannot be expected. In addition, the problem related to the voids formation in the contact filling process as mentioned above still remains.

Please replace the paragraph beginning at page 14, line 20, with the following rewritten paragraph:

In Fig. 6, a phase-change memory device structure according to a preferred embodiment of the present invention is exemplified. An FET 590 is formed below a phase-change resistor 550 through a conventional CMOS process technology. In the structure, ~~1~~ one memory cell includes ~~1~~ one FET and ~~1~~ one phase-change resistor. The structure below the phase-change resistor 550 can be variously modified in accordance with the specification which is required to meet in each of the detailed applications. For an example of the modifications, a LOCOS (Local Oxidation of Silicon) structure can replace the STI (Shallow Trench Isolation) structure 510 shown in Fig. 6 as a device isolation structure. For another example of the modifications, another type of switching device such as a BJT (Bipolar Junction Transistor) can ~~replaced~~ replace the FET 590 employed in the structure of Fig. 6. Therefore, the embodiment shown in Fig. 6 should be considered as an example.

Please replace the paragraph beginning at page 16, line 2, with the following rewritten paragraph:

In Fig. 7, is shown a structure of a phase-change memory device according to another preferred embodiment of the present invention. In that structure, PN diodes 690 are formed on substructures 610 and below phase-change resistors 650 instead of the CMOS structure of Fig. 6. As mentioned above, that change can be considered as a modification of design by those skilled in the art. In the structure of Fig. 7, there are ~~there~~ a lower dielectric layer 635, a contact hole 640 formed in the lower dielectric layer 635, a lower electrode 645 filling the contact hole 640, a thin dielectric layer 637 which ~~cover~~ covers the top surface of the lower electrode 645 and the top surface of the lower dielectric layer 635. The phase-change resistor 650 contacts to the lower electrode 645 electrically through a micro pore 648 formed in the thin dielectric layer 637, which provides a local current path.

Please replace the paragraph beginning at page 18, line 17, with the following rewritten paragraph:

As drawn in (d), the top surface of the lower electrode 745 and the top surface of the lower dielectric layer ~~737~~ 735 are covered with a thin dielectric layer 737 after removing the mask 746. Then, a mask material film 780 is coated and a patterning process is performed as shown in (e). For the mask material film 780, a photo resist layer or a polymer layer can be used. The mask material can be chosen according to the lithography process. To obtain the micro pore or the damaged spot which has much smaller dimension than the top surface of the lower electrode, the exposed bottom area in the pattern should be much smaller than the top surface area of lower electrode as shown in (f). Therefore, e-beam lithography or nano-imprinting lithography which will be further explained below is ideal for obtaining the small sized pattern as mentioned above.

Please replace the paragraph beginning at page 20, line 33, with the following rewritten paragraph:

As explained above, the structure of the phase-change memory device proposed in the present invention can provide a very advantageous effect in consideration of the overlay margin of the lithographic processes. Fig. 12 is a drawing for explaining the effect of the enhanced overlay margin by using the proposed structure. As shown in Fig. 12, the proposed structure employing the micro pores provides large overlay margin even in ~~case~~

~~that~~ cases where the lower electrodes 945 have vertical sidewalls thus providing reliability of manufacturing processes and enhancing productivity. In ~~case that~~ cases where the lower electrodes 845 have tapered sidewalls as shown in Fig. 15, the overlay margin can be enhanced more because the top surface area of the lower electrode 845 is larger. Also in the structure of Fig. 15, the recessed regions having tapered sidewalls in the lower dielectric layer can be easily filled with metallic materials avoiding voids and ~~seems~~ seams, and the lower electrodes ~~having~~ with good electrical properties can be obtained.